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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,727	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 1-16 rejected under 35 U.S.C. 101 because claims in question appear to be directed to an abstract idea rather than a practical application of the idea. The claimsed invention does not result in physical transformation nor does the claimed invention appear to provide a useful, concrete and tangible result. Specifically, the claimed invention does not appear to produce a tangible result because merely determining two timing signals being out of phase and adjustment of frequency of the first signal to the frequency of the second timing signal are nothing more than a phase tracking functionality. It fails to use or make available for use the result of phase tracking and to enable its functionality and usefulness to be realized. Additionally, the asserted practical application in the specification of the solving of seaming effects and synchronization for displayed and projected image arrays is explained; however the practical application is not explicitly recited in the claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,831,648 B2 to Mukherjee et al. in view of US 5,977,989 to Lee et al.

a. Regarding claim 1, Mukherjee et al. **discloses** synchronizing rendering and display of images across multiple display devices; master system 107 is used to synchronize the rendering and display functions of slave systems 105A and 105B. Synchronization signal generator 120 provides a clock signal and the timing signal is implemented using a plurality of daughter cards 112 (...A timing signal provider for propagating a time synchronization signal is also included within each slave system 105. In one embodiment, the timing signal provider is implemented using a plurality of daughter cards 112. Each daughter card 112 is an integrated circuit board used for providing external clock synchronization between the slave systems 105 and master system 107. In the case where multiple daughter cards 112 are used within an individual slave system 105, then the daughter cards 112 can be connected to one another in a daisy chain...col. 3, lines 31-43). These daughter cards 112 extract the timing signal and pass it on to the graphics processors 110. This timing signal would be used to provide clock synchronization between the master system 107 and the slave systems 105A and 105B. A first graphics processing unit is similar to Mukherjee's master system 107 and a second graphics processing unit is similar to the slave system 105A, 105B. However, Mukherjee et al. **does not explicitly disclose** synchronizing or "genlocking" signals from different sources in terms of phase comparison. Lee et al. **discloses** synchronization between two sources of video data which are running at a different clock frequency or at the same clock frequency but at different phases (...Since the pixel data from video processor 126 may be running at a different clock frequency or phase than the data from graphics processor 108, there is a need to provide synchronization between the two sources of data. The synchronization between two sources of video data which are running at a different clock frequency or at the same clock frequency but at different phases, is called genlocking. Video processor 126 produces an adjustable

vertical sync signal which is input to graphics processor 108 and is also driven to video monitor 114...col. 4, lines 18-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Mukherjee et al. with the feature "synchronizing two timing signal by genlocking their phases" as taught by Lee et al. **because** this helps in improving artifacts due to phase differences in displaying images.

b. Regarding claim 2, Mukherjee et al. further comprising transmitting the synchronized timing signal to a third graphics processing unit (...this timing signal would be used to provide clock synchronization between the master system 107 and the slave systems 105A and **105B**...col. 4, lines 15-18).

c. Regarding claim 15, Mukherjee et al. **discloses** providing a clock signal from a clock generator (synchronization signal generator 120) and an external synchronization signal (...each daughter 112 is an integrated circuit board used for providing external clock synchronization between the slave systems 105 and master system 107...col. 3, lines 34-38). However, Mukherjee et al. **does not explicitly disclose** synchronizing or "genlocking" signals from different sources in terms of phase comparison. Lee et al. **discloses** synchronization between two sources of video data which are running at a different clock frequency or at the same clock frequency but at different phases (...Since the pixel data from video processor 126 may be running at a different clock frequency or phase than the data from graphics processor 108, there is a need to provide synchronization between the two sources of data. The synchronization between two sources of video data which are running at a different clock frequency or at the same clock frequency but at different phases, is called genlocking. Video processor 126 produces an adjustable vertical sync signal which is input to graphics processor 108 and is also driven to video monitor 114...col. 4, lines 18-27). Therefore, it would have been

obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Mukherjee et al. with the feature "synchronizing two timing signal by genlocking their phases" as taught by Lee et al. **because** this helps in improving artifacts due to phase differences in displaying images.

d. Regarding claim 16, it is similar in scope to claim 2 above and is rejected under the same rationale.

4. Claims 3-13, 17-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,831,648 B2 to Mukherjee et al. in view of US 5,977,989 to Lee et al. as applied to claim 1 above, and further in view of US 2004/0012600 A1 to Deering et al.

a. Regarding claim 3, Mukherjee-Lee combination **does not disclose** determining whether a first stereo field signal of the first graphics processing unit and a second stereo field signal of the second graphics processing unit are synchronized; and adjusting the phase of the first stereo field signal to the phase of the second stereo field signal if the first stereo field signal and the second stereo field signal are not synchronized. Deering et al. **discloses** stereo field video signal (...In field sequential stereo video signal formats, there are two sequential fields to each frame. The first field caries the complete image for the left eye; the second field carries the complete image for the right eye. These two images may be shown as sent, e.g., in rapid fashion, with some form of shutter glasses or polarization or image angle of view spatial separation effect on the perception of the video image on the physical image display device of the human(s) viewing the display. In this manner, only (or mostly) the left image will be visible to the left eyes of the human(s) watching, and only (or mostly) the right image will be visible to the right eyes of the human(s) watching, giving rise to perception of stereoscopic depth...paragraph 0386). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by

Mukherjee-Lee combination with the feature "adjusting phases of the first and second stereo field signal for synchronization" as taught by Deering et al. **because** this helps in reducing/eliminating artifacts due to phase differences in displaying images.

b. Regarding claim 4, it is similar in scope to claim 2 above as it involves transmitting the "synchronized stereo field signal" , a video signal that has been synchronized, to a third graphics processing unit disclosed by Mukherjee et al. (...this timing signal would be used to provide clock synchronization between the master system 107 and the slave systems 105A and **105B**...col. 4, lines 15-18).

c. Regarding claim 5, Mukherjee as modified by Lee et al. **discloses** synchronizing a swap ready signal of the first graphics processing unit with a swap ready signal of the second graphics processing unit (...In a multiple processing environment, it is necessary to make sure that each slave system has its graphics processors perform buffer swapping at approximately the same time. Buffer swapping is normally performed during the time of vertical retrace just described. However, despite the close synchronization of vertical retrace among the several slave systems, steps still need to be taken to synchronize frame buffer swapping among the plurality of slave systems, else the display will be synchronized but the data displayed will be out of sync...col.8, lines 8-16; col. 8, lines 56-65).

a. Regarding claim 6, the triggering of a new video start address in a memory are taught **implicitly** by Mukherjee et al. in that buffer swapping is performed during the time of vertical retrace; synchronization module 115 determines when all slave systems 105 are swap ready. Fig. 7 discloses synchronized frame buffer swapping wherein each frame displayed in a scene is proceeded and followed by a vertical interrupt; and while one frame is being displayed another is being rendered by the graphics processors (col. 9. line 10-15). As disclosed, there are two frames and therefore if one frame is being

rendered, it would be obvious that the second frame would be at a different address "triggering a new video start address in a memory". Mukherjee et al. **discloses** determination of a swap ready element on at least one of the graphics processing units is logically true (...Generally, swap ready status is determined by the transmission of either a high or low signal. If the signal is high then the processor has completed rendering the current buffer and is ready to switch. If the signal is low then rendering is still in progress. In a graphics system comprised of multiple graphic processors, each signal contributes to the overall status of the system. Accordingly, if any one graphics processor is not ready, then the signal transmitted will be low...col. 8, lines 66-67; col. 9, lines 1-7). However, Mukherjee et al. **does not disclose** reception of a frame divider. Deering et al. **discloses** for field sequential stereo video signal formats, there are two sequential fields to each frame, the first field carries the complete image for the left eye, the second field carries the complete image for the right eye. This is in addition to the front buffer and back buffers that are swapped. Thus, Deering et al. **implicitly discloses** a frame divider that would separate the front buffer and back buffer. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Mukherjee with the feature "handling of sequential stereo video signal format with two sequential fields that required frame division" as taught by Deering et al. **because** it prevents frame tearing.

b. Regarding claim 7, Mukherjee et al. **implicitly discloses** further comprising scanning out data from the memory starting at the new video start address if the swap ready element on the at least one of the graphics processing units is logically true as the buffer swapping involves scanning out data from the back buffer which will be at a new address, that is inherent in front and back buffer operations and swap ready status is

being reported as being high or low (...Generally, swap ready status is determined by the transmission of either a high or low signal...col. 8, lines 66-67; col. 9, lines 1-10).

c. Regarding claim 8, Mukherjee et al. **discloses** buffer swapping being performed during the time of video blanking interval (vertical retrace)(...Buffer swapping is normally performed during the time of vertical retrace...col. 8, lines 9-11) and based on Swap ready status, the back buffer is then scanned out (...in step 625, synchronization module 115 will determine when all slave systems 105 are swap ready. Once all slave systems 107 have communicated a swap status indicating that they have completed rendering and are swap ready, in a step 630, synchronization module 115 will cause master system 107 to send a broadcast swap command to each slave system 105 over multidrop cable 116...col. 8, lines 56-63).

d. Regarding claim 9, it is similar in scope to claim 7 above and is rejected under the same rationale.

e. Regarding claim 10, it is similar in scope to claim 8 above and is rejected under the same rationale.

f. Regarding claim 11, Mukherjee et al. **discloses** wherein the swap ready element is logically true when an image content stored in a back portion of a frame buffer in the at least one of the graphics processing units is ready to be transferred to a front portion of the frame buffer (...In a step 625, synchronization module 115 will determine when all slave systems 105 are swap ready. Once all slave systems 107 have communicated a swap status indicating that they have completed rendering and are swap ready, in a step 630, synchronization module 115 will cause master system 107 to send a broadcast swap command to each slave system 105 over multidrop cable 116...col. 8, lines 56-65).

g. Regarding claims 12 and 13, Mukherjee et al. **discloses** swap ready status is determined by the transmission of either a high or low signal (...Generally, swap ready

status is determined by the transmission of either a high or low signal. If the signal is high then the processor has completed rendering the current buffer and is ready to switch. If the signal is low the rendering is still in progress...col. 8, lines 65-67; col. 9, lines 1-5).

h. Regarding claim 17, it is similar in scope to claim 7 above and is rejected under the same rationale.

i. Regarding claim 18, Murkherjee et al. **discloses** that buffer swapping is normally performed during the time of vertical retrace. Therefore, suspension of rendering in response to frame divider in inherent.

j. Regarding claim 19, it is similar in scope to claim 8 above and is rejected under the same rationale.

k. Regarding claim 20, it is similar in scope to claim 11 above and is rejected under the same rationale.

l. Regarding claims 21 and 22, they are similar to claims 12 and 13 respectively and are rejected under the same rationale.

m. Regarding claim 23, in a graphics processing system, frames are continuously being scanned out to the display and therefore it is inherent for method to be repeated for successive frames.

n. Regarding claim 24, it is similar in scope to claim 17 above and is rejected under the same rationale.

o. Regarding claim 25, it is similar in scope to claim 18 above and is rejected under the same rationale.

p. Regarding claim 26, it is similar in scope to claim 19 above and is rejected under the same rationale.

q. Regarding claim 27, it is similar in scope to claim 20 above and is rejected under the same rationale.

r. Regarding claims 28 and 29, they are similar in scope to claims 21 and 22 respectively and are rejected under the same rationale.

s. Regarding claim 30, is similar in scope to claim 25 above and is rejected under the same rationale.

t. Regarding claim 31, it is similar in scope to claim 1 above and is rejected under the same rationale.

u. Regarding claim 32, it is similar in scope to claim 3 above and is rejected under the same rationale.

v. Regarding claim 33, it is similar in scope to claim 5 above and is rejected under the same rationale.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,831,648 B2 to Mukherjee et al. in view of US 5,977,989 to Lee et al. as applied to claim 1 above, and further in view of US 5,638,531 to Crump et al.

a. Regarding claim 15, Mukherjee-Crump combination **does not disclose** wherein the first graphics processing unit and the second processing unit are implemented on one of a silicon substrate, a printed circuit board, and an array of display elements. Crump et al. **discloses** a parallel video processing system onto a Very Large Scale Integrated (VLSI) device (...Each of a plurality of processors (indicated at 30a, 30b, 30c and 30d in FIG. 3)...col. 3, lines 23-30). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Mukharjee-Lee combination with the feature "plurality of graphics processing units on a silicon substrate" as taught by Crump et al. **because** both processing units

being on a common, single substrate allows for higher bandwidth communication between the processors and memory (col. 3, lines 45-47).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:00AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh

Examiner, Art Unit 2628

dks

September 29, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER